Route design – timing summary

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| Tool Version : Vivado v.2021.1 (win64) Build 3247384 Thu Jun 10 19:36:33 MDT 2021

| Date : Wed Apr 10 16:12:18 2024

| Host : DESKTOP-4LK3EFH running 64-bit major release (build 9200)

| Command : report\_timing\_summary -max\_paths 10 -file UART\_timing\_summary\_routed.rpt -pb UART\_timing\_summary\_routed.pb -rpx UART\_timing\_summary\_routed.rpx -warn\_on\_violation

| Design : UART

| Device : 7z020-clg400

| Speed File : -1 PRODUCTION 1.12 2019-11-22

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Timing Summary Report

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| Timer Settings

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Enable Multi Corner Analysis : Yes

Enable Pessimism Removal : Yes

Pessimism Removal Resolution : Nearest Common Node

Enable Input Delay Default Clock : No

Enable Preset / Clear Arcs : No

Disable Flight Delays : No

Ignore I/O Paths : No

Timing Early Launch at Borrowing Latches : No

Borrow Time for Max Delay Exceptions : Yes

Merge Timing Exceptions : Yes

Corner Analyze Analyze

Name Max Paths Min Paths

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Slow Yes Yes

Fast Yes Yes

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| Report Methodology

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Rule Severity Description Violations

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TIMING-18 Warning Missing input or output delay 19

ULMTCS-2 Warning Control Sets use limits require reduction 1

Note: This report is based on the most recent report\_methodology run and may not be up-to-date. Run report\_methodology on the current design for the latest report.

check\_timing report

Table of Contents

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1. checking no\_clock (0)

2. checking constant\_clock (0)

3. checking pulse\_width\_clock (0)

4. checking unconstrained\_internal\_endpoints (0)

5. checking no\_input\_delay (11)

6. checking no\_output\_delay (8)

7. checking multiple\_clock (0)

8. checking generated\_clocks (0)

9. checking loops (0)

10. checking partial\_input\_delay (0)

11. checking partial\_output\_delay (0)

12. checking latch\_loops (0)

1. checking no\_clock (0)

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There are 0 register/latch pins with no clock.

2. checking constant\_clock (0)

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There are 0 register/latch pins with constant\_clock.

3. checking pulse\_width\_clock (0)

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There are 0 register/latch pins which need pulse\_width check

4. checking unconstrained\_internal\_endpoints (0)

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There are 0 pins that are not constrained for maximum delay.

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no\_input\_delay (11)

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There are 11 input ports with no input delay specified. (HIGH)

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no\_output\_delay (8)

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There are 8 ports with no output delay specified. (HIGH)

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple\_clock (0)

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There are 0 register/latch pins with multiple clocks.

8. checking generated\_clocks (0)

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There are 0 generated clocks that are not connected to a clock source.

9. checking loops (0)

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There are 0 combinational loops in the design.

10. checking partial\_input\_delay (0)

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There are 0 input ports with partial input delay specified.

11. checking partial\_output\_delay (0)

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There are 0 ports with partial output delay specified.

12. checking latch\_loops (0)

----------------------------

There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary

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WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

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0.891 0.000 0 25218 0.059 0.000 0 25218 3.500 0.000 0 16717

All user specified timing constraints are met.

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| Clock Summary

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Clock Waveform(ns) Period(ns) Frequency(MHz)

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sys\_clk\_pin {0.000 4.000} 10.000 100.000

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| Intra Clock Table

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Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

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sys\_clk\_pin 0.891 0.000 0 25218 0.059 0.000 0 25218 3.500 0.000 0 16717

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| Inter Clock Table

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From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints

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| Other Path Groups Table

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Path Group From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints

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| Timing Details

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From Clock: sys\_clk\_pin

To Clock: sys\_clk\_pin

Setup : 0 Failing Endpoints, Worst Slack 0.891ns, Total Violation 0.000ns

Hold : 0 Failing Endpoints, Worst Slack 0.059ns, Total Violation 0.000ns

PW : 0 Failing Endpoints, Worst Slack 3.500ns, Total Violation 0.000ns

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Max Delay Paths

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Slack (MET) : 0.891ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[611][1]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.683ns (logic 1.500ns (17.275%) route 7.183ns (82.725%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: 0.018ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.414ns = ( 15.414 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.424ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

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SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 11.359 f fifo\_tx/mem[639][7]\_i\_2\_\_0/O

net (fo=109, routed) 1.967 13.327 fifo\_tx/mem[639][7]\_i\_2\_\_0\_n\_0

SLICE\_X92Y7 LUT5 (Prop\_lut5\_I4\_O) 0.150 13.477 r fifo\_tx/mem[611][7]\_i\_1\_\_0/O

net (fo=8, routed) 1.026 14.503 fifo\_tx/mem[611][7]\_i\_1\_\_0\_n\_0

SLICE\_X103Y4 FDRE r fifo\_tx/mem\_reg[611][1]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.625 15.414 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X103Y4 FDRE r fifo\_tx/mem\_reg[611][1]/C

clock pessimism 0.424 15.838

clock uncertainty -0.035 15.802

SLICE\_X103Y4 FDRE (Setup\_fdre\_C\_CE) -0.409 15.393 fifo\_tx/mem\_reg[611][1]

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required time 15.393

arrival time -14.503

-------------------------------------------------------------------

slack 0.891

Slack (MET) : 0.891ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[611][5]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.683ns (logic 1.500ns (17.275%) route 7.183ns (82.725%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: 0.018ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.414ns = ( 15.414 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.424ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

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(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

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net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

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SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

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net (fo=109, routed) 1.967 13.327 fifo\_tx/mem[639][7]\_i\_2\_\_0\_n\_0

SLICE\_X92Y7 LUT5 (Prop\_lut5\_I4\_O) 0.150 13.477 r fifo\_tx/mem[611][7]\_i\_1\_\_0/O

net (fo=8, routed) 1.026 14.503 fifo\_tx/mem[611][7]\_i\_1\_\_0\_n\_0

SLICE\_X103Y4 FDRE r fifo\_tx/mem\_reg[611][5]/CE

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(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.625 15.414 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X103Y4 FDRE r fifo\_tx/mem\_reg[611][5]/C

clock pessimism 0.424 15.838

clock uncertainty -0.035 15.802

SLICE\_X103Y4 FDRE (Setup\_fdre\_C\_CE) -0.409 15.393 fifo\_tx/mem\_reg[611][5]

-------------------------------------------------------------------

required time 15.393

arrival time -14.503

-------------------------------------------------------------------

slack 0.891

Slack (MET) : 0.924ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[797][4]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.659ns (logic 1.674ns (19.332%) route 6.985ns (80.668%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.213ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.284ns = ( 15.284 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.354 12.706 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X56Y3 LUT5 (Prop\_lut5\_I4\_O) 0.331 13.037 r fifo\_tx/mem[797][7]\_i\_1\_\_0/O

net (fo=8, routed) 1.442 14.479 fifo\_tx/mem[797][7]\_i\_1\_\_0\_n\_0

SLICE\_X32Y4 FDRE r fifo\_tx/mem\_reg[797][4]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.495 15.284 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X32Y4 FDRE r fifo\_tx/mem\_reg[797][4]/C

clock pessimism 0.323 15.607

clock uncertainty -0.035 15.572

SLICE\_X32Y4 FDRE (Setup\_fdre\_C\_CE) -0.169 15.403 fifo\_tx/mem\_reg[797][4]

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required time 15.403

arrival time -14.479

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slack 0.924

Slack (MET) : 0.928ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[885][4]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.485ns (logic 1.669ns (19.670%) route 6.816ns (80.330%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.139ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.358ns = ( 15.358 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.668 13.021 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X41Y12 LUT5 (Prop\_lut5\_I4\_O) 0.326 13.347 r fifo\_tx/mem[885][7]\_i\_1\_\_0/O

net (fo=8, routed) 0.958 14.305 fifo\_tx/mem[885][7]\_i\_1\_\_0\_n\_0

SLICE\_X31Y10 FDRE r fifo\_tx/mem\_reg[885][4]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.569 15.358 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X31Y10 FDRE r fifo\_tx/mem\_reg[885][4]/C

clock pessimism 0.323 15.681

clock uncertainty -0.035 15.646

SLICE\_X31Y10 FDRE (Setup\_fdre\_C\_CE) -0.413 15.233 fifo\_tx/mem\_reg[885][4]

-------------------------------------------------------------------

required time 15.233

arrival time -14.305

-------------------------------------------------------------------

slack 0.928

Slack (MET) : 0.972ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[890][2]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.370ns (logic 1.670ns (19.953%) route 6.700ns (80.047%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.215ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.282ns = ( 15.282 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.648 13.001 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X41Y12 LUT5 (Prop\_lut5\_I4\_O) 0.327 13.328 r fifo\_tx/mem[890][7]\_i\_1\_\_0/O

net (fo=8, routed) 0.862 14.190 fifo\_tx/mem[890][7]\_i\_1\_\_0\_n\_0

SLICE\_X33Y9 FDRE r fifo\_tx/mem\_reg[890][2]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.493 15.282 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X33Y9 FDRE r fifo\_tx/mem\_reg[890][2]/C

clock pessimism 0.323 15.605

clock uncertainty -0.035 15.570

SLICE\_X33Y9 FDRE (Setup\_fdre\_C\_CE) -0.408 15.162 fifo\_tx/mem\_reg[890][2]

-------------------------------------------------------------------

required time 15.162

arrival time -14.190

-------------------------------------------------------------------

slack 0.972

Slack (MET) : 0.974ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[885][2]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.399ns (logic 1.669ns (19.871%) route 6.730ns (80.129%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.215ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.282ns = ( 15.282 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.668 13.021 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X41Y12 LUT5 (Prop\_lut5\_I4\_O) 0.326 13.347 r fifo\_tx/mem[885][7]\_i\_1\_\_0/O

net (fo=8, routed) 0.873 14.219 fifo\_tx/mem[885][7]\_i\_1\_\_0\_n\_0

SLICE\_X32Y9 FDRE r fifo\_tx/mem\_reg[885][2]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.493 15.282 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X32Y9 FDRE r fifo\_tx/mem\_reg[885][2]/C

clock pessimism 0.323 15.605

clock uncertainty -0.035 15.570

SLICE\_X32Y9 FDRE (Setup\_fdre\_C\_CE) -0.377 15.193 fifo\_tx/mem\_reg[885][2]

-------------------------------------------------------------------

required time 15.193

arrival time -14.219

-------------------------------------------------------------------

slack 0.974

Slack (MET) : 0.974ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[885][6]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.399ns (logic 1.669ns (19.871%) route 6.730ns (80.129%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.215ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.282ns = ( 15.282 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.668 13.021 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X41Y12 LUT5 (Prop\_lut5\_I4\_O) 0.326 13.347 r fifo\_tx/mem[885][7]\_i\_1\_\_0/O

net (fo=8, routed) 0.873 14.219 fifo\_tx/mem[885][7]\_i\_1\_\_0\_n\_0

SLICE\_X32Y9 FDRE r fifo\_tx/mem\_reg[885][6]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.493 15.282 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X32Y9 FDRE r fifo\_tx/mem\_reg[885][6]/C

clock pessimism 0.323 15.605

clock uncertainty -0.035 15.570

SLICE\_X32Y9 FDRE (Setup\_fdre\_C\_CE) -0.377 15.193 fifo\_tx/mem\_reg[885][6]

-------------------------------------------------------------------

required time 15.193

arrival time -14.219

-------------------------------------------------------------------

slack 0.974

Slack (MET) : 0.977ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[790][4]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.607ns (logic 1.674ns (19.450%) route 6.933ns (80.550%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.212ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.285ns = ( 15.285 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.180 11.235 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y23 LUT4 (Prop\_lut4\_I1\_O) 0.117 11.352 f fifo\_tx/mem[959][7]\_i\_2\_\_0/O

net (fo=113, routed) 1.357 12.709 fifo\_tx/mem[959][7]\_i\_2\_\_0\_n\_0

SLICE\_X54Y3 LUT5 (Prop\_lut5\_I4\_O) 0.331 13.040 r fifo\_tx/mem[790][7]\_i\_1\_\_0/O

net (fo=8, routed) 1.386 14.427 fifo\_tx/mem[790][7]\_i\_1\_\_0\_n\_0

SLICE\_X34Y4 FDRE r fifo\_tx/mem\_reg[790][4]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.496 15.285 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X34Y4 FDRE r fifo\_tx/mem\_reg[790][4]/C

clock pessimism 0.323 15.608

clock uncertainty -0.035 15.573

SLICE\_X34Y4 FDRE (Setup\_fdre\_C\_CE) -0.169 15.404 fifo\_tx/mem\_reg[790][4]

-------------------------------------------------------------------

required time 15.404

arrival time -14.427

-------------------------------------------------------------------

slack 0.977

Slack (MET) : 0.977ns (required time - arrival time)

Source: fifo\_tx/w\_ptr\_reg[2]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_tx/mem\_reg[399][1]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.738ns (logic 1.474ns (16.868%) route 7.264ns (83.132%))

Logic Levels: 6 (CARRY4=1 LUT4=2 LUT5=1 LUT6=2)

Clock Path Skew: -0.044ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.352ns = ( 15.352 - 10.000 )

Source Clock Delay (SCD): 5.820ns

Clock Pessimism Removal (CPR): 0.424ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.722 5.820 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X63Y32 FDRE r fifo\_tx/w\_ptr\_reg[2]/C

------------------------------------------------------------------- -------------------

SLICE\_X63Y32 FDRE (Prop\_fdre\_C\_Q) 0.456 6.276 r fifo\_tx/w\_ptr\_reg[2]/Q

net (fo=94, routed) 1.625 7.901 fifo\_tx/w\_ptr\_reg[2]

SLICE\_X66Y16 LUT6 (Prop\_lut6\_I0\_O) 0.124 8.025 r fifo\_tx/mem[1023][7]\_i\_2\_\_0/O

net (fo=32, routed) 0.662 8.688 fifo\_tx/mem[1023][7]\_i\_2\_\_0\_n\_0

SLICE\_X64Y23 LUT4 (Prop\_lut4\_I1\_O) 0.124 8.812 r fifo\_tx/w\_ptr[8]\_i\_1\_\_0/O

net (fo=9, routed) 0.722 9.533 fifo\_tx/w\_ptr0\_\_0[8]

SLICE\_X64Y29 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.657 r fifo\_tx/w\_ptr[9]\_i\_5/O

net (fo=1, routed) 0.000 9.657 fifo\_tx/w\_ptr[9]\_i\_5\_n\_0

SLICE\_X64Y29 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.055 f fifo\_tx/w\_ptr\_reg[9]\_i\_3/CO[3]

net (fo=17, routed) 1.173 11.228 fifo\_tx/w\_ptr\_reg[9]\_i\_3\_n\_0

SLICE\_X66Y24 LUT4 (Prop\_lut4\_I2\_O) 0.124 11.352 f fifo\_tx/mem[511][7]\_i\_2\_\_0/O

net (fo=190, routed) 2.086 13.438 fifo\_tx/mem[511][7]\_i\_2\_\_0\_n\_0

SLICE\_X94Y39 LUT5 (Prop\_lut5\_I1\_O) 0.124 13.562 r fifo\_tx/mem[399][7]\_i\_1\_\_0/O

net (fo=8, routed) 0.996 14.558 fifo\_tx/mem[399][7]\_i\_1\_\_0\_n\_0

SLICE\_X87Y43 FDRE r fifo\_tx/mem\_reg[399][1]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.563 15.352 fifo\_tx/clk\_IBUF\_BUFG

SLICE\_X87Y43 FDRE r fifo\_tx/mem\_reg[399][1]/C

clock pessimism 0.424 15.776

clock uncertainty -0.035 15.740

SLICE\_X87Y43 FDRE (Setup\_fdre\_C\_CE) -0.205 15.535 fifo\_tx/mem\_reg[399][1]

-------------------------------------------------------------------

required time 15.535

arrival time -14.558

-------------------------------------------------------------------

slack 0.977

Slack (MET) : 0.979ns (required time - arrival time)

Source: fifo\_rx/w\_ptr\_reg[1]/C

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[31][2]/CE

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys\_clk\_pin rise@10.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 8.337ns (logic 1.498ns (17.967%) route 6.839ns (82.033%))

Logic Levels: 6 (CARRY4=1 LUT4=1 LUT5=1 LUT6=3)

Clock Path Skew: -0.239ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.256ns = ( 15.256 - 10.000 )

Source Clock Delay (SCD): 5.819ns

Clock Pessimism Removal (CPR): 0.323ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.475 1.475 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.522 3.997 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.101 4.098 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.721 5.819 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X80Y93 FDRE r fifo\_rx/w\_ptr\_reg[1]/C

------------------------------------------------------------------- -------------------

SLICE\_X80Y93 FDRE (Prop\_fdre\_C\_Q) 0.456 6.275 r fifo\_rx/w\_ptr\_reg[1]/Q

net (fo=101, routed) 1.674 7.948 fifo\_rx/w\_ptr\_reg[1]

SLICE\_X54Y103 LUT6 (Prop\_lut6\_I2\_O) 0.124 8.072 r fifo\_rx/mem[1023][7]\_i\_2/O

net (fo=25, routed) 0.850 8.922 fifo\_rx/mem[1023][7]\_i\_2\_n\_0

SLICE\_X51Y105 LUT4 (Prop\_lut4\_I1\_O) 0.124 9.046 r fifo\_rx/w\_ptr[8]\_i\_1/O

net (fo=6, routed) 0.453 9.500 fifo\_rx/w\_ptr0\_\_0[8]

SLICE\_X52Y106 LUT6 (Prop\_lut6\_I1\_O) 0.124 9.624 r fifo\_rx/mem[0][7]\_i\_6/O

net (fo=1, routed) 0.000 9.624 fifo\_rx/mem[0][7]\_i\_6\_n\_0

SLICE\_X52Y106 CARRY4 (Prop\_carry4\_S[2]\_CO[3])

0.398 10.022 f fifo\_rx/mem\_reg[0][7]\_i\_3/CO[3]

net (fo=22, routed) 1.808 11.830 fifo\_rx/CO[0]

SLICE\_X45Y83 LUT6 (Prop\_lut6\_I2\_O) 0.124 11.954 r fifo\_rx/mem[63][7]\_i\_2/O

net (fo=45, routed) 1.376 13.330 fifo\_rx/mem[63][7]\_i\_2\_n\_0

SLICE\_X38Y70 LUT5 (Prop\_lut5\_I3\_O) 0.148 13.478 r fifo\_rx/mem[31][7]\_i\_1/O

net (fo=8, routed) 0.678 14.156 fifo\_rx/mem[31][7]\_i\_1\_n\_0

SLICE\_X41Y69 FDRE r fifo\_rx/mem\_reg[31][2]/CE

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

10.000 10.000 r

K17 0.000 10.000 r clk (IN)

net (fo=0) 0.000 10.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 1.404 11.404 r clk\_IBUF\_inst/O

net (fo=1, routed) 2.293 13.697 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.091 13.788 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 1.468 15.256 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X41Y69 FDRE r fifo\_rx/mem\_reg[31][2]/C

clock pessimism 0.323 15.580

clock uncertainty -0.035 15.544

SLICE\_X41Y69 FDRE (Setup\_fdre\_C\_CE) -0.409 15.135 fifo\_rx/mem\_reg[31][2]

-------------------------------------------------------------------

required time 15.135

arrival time -14.156

-------------------------------------------------------------------

slack 0.979

Min Delay Paths

--------------------------------------------------------------------------------------

Slack (MET) : 0.059ns (arrival time - required time)

Source: receiver/b\_reg\_reg[7]\_rep\_\_3/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[755][7]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.389ns (logic 0.141ns (36.263%) route 0.248ns (63.737%))

Logic Levels: 0

Clock Path Skew: 0.258ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.260ns

Source Clock Delay (SCD): 1.736ns

Clock Pessimism Removal (CPR): 0.265ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.626 1.736 receiver/clk\_IBUF\_BUFG

SLICE\_X45Y126 FDCE r receiver/b\_reg\_reg[7]\_rep\_\_3/C

------------------------------------------------------------------- -------------------

SLICE\_X45Y126 FDCE (Prop\_fdce\_C\_Q) 0.141 1.877 r receiver/b\_reg\_reg[7]\_rep\_\_3/Q

net (fo=64, routed) 0.248 2.125 fifo\_rx/mem\_reg[705][7]\_0[7]

SLICE\_X51Y127 FDRE r fifo\_rx/mem\_reg[755][7]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.893 2.260 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X51Y127 FDRE r fifo\_rx/mem\_reg[755][7]/C

clock pessimism -0.265 1.995

SLICE\_X51Y127 FDRE (Hold\_fdre\_C\_D) 0.072 2.067 fifo\_rx/mem\_reg[755][7]

-------------------------------------------------------------------

required time -2.067

arrival time 2.125

-------------------------------------------------------------------

slack 0.059

Slack (MET) : 0.063ns (arrival time - required time)

Source: receiver/b\_reg\_reg[5]\_rep\_\_0/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[911][5]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.402ns (logic 0.141ns (35.056%) route 0.261ns (64.944%))

Logic Levels: 0

Clock Path Skew: 0.267ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.191ns

Source Clock Delay (SCD): 1.662ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.552 1.662 receiver/clk\_IBUF\_BUFG

SLICE\_X52Y94 FDCE r receiver/b\_reg\_reg[5]\_rep\_\_0/C

------------------------------------------------------------------- -------------------

SLICE\_X52Y94 FDCE (Prop\_fdce\_C\_Q) 0.141 1.803 r receiver/b\_reg\_reg[5]\_rep\_\_0/Q

net (fo=64, routed) 0.261 2.064 fifo\_rx/mem\_reg[897][7]\_0[5]

SLICE\_X49Y95 FDRE r fifo\_rx/mem\_reg[911][5]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.824 2.191 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X49Y95 FDRE r fifo\_rx/mem\_reg[911][5]/C

clock pessimism -0.261 1.929

SLICE\_X49Y95 FDRE (Hold\_fdre\_C\_D) 0.072 2.001 fifo\_rx/mem\_reg[911][5]

-------------------------------------------------------------------

required time -2.001

arrival time 2.064

-------------------------------------------------------------------

slack 0.063

Slack (MET) : 0.065ns (arrival time - required time)

Source: receiver/b\_reg\_reg[5]\_rep\_\_0/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[896][5]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.403ns (logic 0.141ns (34.964%) route 0.262ns (65.036%))

Logic Levels: 0

Clock Path Skew: 0.267ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.191ns

Source Clock Delay (SCD): 1.662ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.552 1.662 receiver/clk\_IBUF\_BUFG

SLICE\_X52Y94 FDCE r receiver/b\_reg\_reg[5]\_rep\_\_0/C

------------------------------------------------------------------- -------------------

SLICE\_X52Y94 FDCE (Prop\_fdce\_C\_Q) 0.141 1.803 r receiver/b\_reg\_reg[5]\_rep\_\_0/Q

net (fo=64, routed) 0.262 2.065 fifo\_rx/mem\_reg[897][7]\_0[5]

SLICE\_X49Y96 FDRE r fifo\_rx/mem\_reg[896][5]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.824 2.191 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X49Y96 FDRE r fifo\_rx/mem\_reg[896][5]/C

clock pessimism -0.261 1.929

SLICE\_X49Y96 FDRE (Hold\_fdre\_C\_D) 0.071 2.000 fifo\_rx/mem\_reg[896][5]

-------------------------------------------------------------------

required time -2.000

arrival time 2.065

-------------------------------------------------------------------

slack 0.065

Slack (MET) : 0.079ns (arrival time - required time)

Source: receiver/b\_reg\_reg[2]\_rep\_\_1/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[788][2]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.404ns (logic 0.141ns (34.869%) route 0.263ns (65.131%))

Logic Levels: 0

Clock Path Skew: 0.259ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.188ns

Source Clock Delay (SCD): 1.667ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.557 1.667 receiver/clk\_IBUF\_BUFG

SLICE\_X44Y97 FDCE r receiver/b\_reg\_reg[2]\_rep\_\_1/C

------------------------------------------------------------------- -------------------

SLICE\_X44Y97 FDCE (Prop\_fdce\_C\_Q) 0.141 1.808 r receiver/b\_reg\_reg[2]\_rep\_\_1/Q

net (fo=64, routed) 0.263 2.071 fifo\_rx/mem\_reg[769][7]\_0[2]

SLICE\_X51Y97 FDRE r fifo\_rx/mem\_reg[788][2]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.821 2.188 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X51Y97 FDRE r fifo\_rx/mem\_reg[788][2]/C

clock pessimism -0.261 1.926

SLICE\_X51Y97 FDRE (Hold\_fdre\_C\_D) 0.066 1.992 fifo\_rx/mem\_reg[788][2]

-------------------------------------------------------------------

required time -1.992

arrival time 2.071

-------------------------------------------------------------------

slack 0.079

Slack (MET) : 0.108ns (arrival time - required time)

Source: receiver/b\_reg\_reg[7]\_rep\_\_2/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[789][7]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.377ns (logic 0.128ns (33.935%) route 0.249ns (66.065%))

Logic Levels: 0

Clock Path Skew: 0.259ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.188ns

Source Clock Delay (SCD): 1.667ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.557 1.667 receiver/clk\_IBUF\_BUFG

SLICE\_X44Y97 FDCE r receiver/b\_reg\_reg[7]\_rep\_\_2/C

------------------------------------------------------------------- -------------------

SLICE\_X44Y97 FDCE (Prop\_fdce\_C\_Q) 0.128 1.795 r receiver/b\_reg\_reg[7]\_rep\_\_2/Q

net (fo=64, routed) 0.249 2.044 fifo\_rx/mem\_reg[769][7]\_0[7]

SLICE\_X50Y97 FDRE r fifo\_rx/mem\_reg[789][7]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.821 2.188 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X50Y97 FDRE r fifo\_rx/mem\_reg[789][7]/C

clock pessimism -0.261 1.926

SLICE\_X50Y97 FDRE (Hold\_fdre\_C\_D) 0.010 1.936 fifo\_rx/mem\_reg[789][7]

-------------------------------------------------------------------

required time -1.936

arrival time 2.044

-------------------------------------------------------------------

slack 0.108

Slack (MET) : 0.116ns (arrival time - required time)

Source: receiver/b\_reg\_reg[3]\_rep\_\_0/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[897][3]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.449ns (logic 0.141ns (31.384%) route 0.308ns (68.616%))

Logic Levels: 0

Clock Path Skew: 0.267ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.191ns

Source Clock Delay (SCD): 1.662ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.552 1.662 receiver/clk\_IBUF\_BUFG

SLICE\_X52Y95 FDCE r receiver/b\_reg\_reg[3]\_rep\_\_0/C

------------------------------------------------------------------- -------------------

SLICE\_X52Y95 FDCE (Prop\_fdce\_C\_Q) 0.141 1.803 r receiver/b\_reg\_reg[3]\_rep\_\_0/Q

net (fo=64, routed) 0.308 2.111 fifo\_rx/mem\_reg[897][7]\_0[3]

SLICE\_X49Y93 FDRE r fifo\_rx/mem\_reg[897][3]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.824 2.191 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X49Y93 FDRE r fifo\_rx/mem\_reg[897][3]/C

clock pessimism -0.261 1.929

SLICE\_X49Y93 FDRE (Hold\_fdre\_C\_D) 0.066 1.995 fifo\_rx/mem\_reg[897][3]

-------------------------------------------------------------------

required time -1.995

arrival time 2.111

-------------------------------------------------------------------

slack 0.116

Slack (MET) : 0.119ns (arrival time - required time)

Source: receiver/b\_reg\_reg[1]\_rep\_\_2/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[754][1]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.434ns (logic 0.164ns (37.796%) route 0.270ns (62.204%))

Logic Levels: 0

Clock Path Skew: 0.256ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.260ns

Source Clock Delay (SCD): 1.738ns

Clock Pessimism Removal (CPR): 0.265ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.628 1.738 receiver/clk\_IBUF\_BUFG

SLICE\_X46Y127 FDCE r receiver/b\_reg\_reg[1]\_rep\_\_2/C

------------------------------------------------------------------- -------------------

SLICE\_X46Y127 FDCE (Prop\_fdce\_C\_Q) 0.164 1.902 r receiver/b\_reg\_reg[1]\_rep\_\_2/Q

net (fo=64, routed) 0.270 2.172 fifo\_rx/mem\_reg[705][7]\_0[1]

SLICE\_X50Y127 FDRE r fifo\_rx/mem\_reg[754][1]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.893 2.260 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X50Y127 FDRE r fifo\_rx/mem\_reg[754][1]/C

clock pessimism -0.265 1.995

SLICE\_X50Y127 FDRE (Hold\_fdre\_C\_D) 0.059 2.054 fifo\_rx/mem\_reg[754][1]

-------------------------------------------------------------------

required time -2.054

arrival time 2.172

-------------------------------------------------------------------

slack 0.119

Slack (MET) : 0.123ns (arrival time - required time)

Source: receiver/b\_reg\_reg[0]\_rep/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[908][0]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.436ns (logic 0.141ns (32.321%) route 0.295ns (67.679%))

Logic Levels: 0

Clock Path Skew: 0.267ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.191ns

Source Clock Delay (SCD): 1.662ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.552 1.662 receiver/clk\_IBUF\_BUFG

SLICE\_X52Y95 FDCE r receiver/b\_reg\_reg[0]\_rep/C

------------------------------------------------------------------- -------------------

SLICE\_X52Y95 FDCE (Prop\_fdce\_C\_Q) 0.141 1.803 r receiver/b\_reg\_reg[0]\_rep/Q

net (fo=64, routed) 0.295 2.098 fifo\_rx/mem\_reg[897][7]\_0[0]

SLICE\_X49Y94 FDRE r fifo\_rx/mem\_reg[908][0]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.824 2.191 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X49Y94 FDRE r fifo\_rx/mem\_reg[908][0]/C

clock pessimism -0.261 1.929

SLICE\_X49Y94 FDRE (Hold\_fdre\_C\_D) 0.046 1.975 fifo\_rx/mem\_reg[908][0]

-------------------------------------------------------------------

required time -1.975

arrival time 2.098

-------------------------------------------------------------------

slack 0.123

Slack (MET) : 0.125ns (arrival time - required time)

Source: receiver/b\_reg\_reg[2]\_rep\_\_1/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[792][2]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.454ns (logic 0.141ns (31.051%) route 0.313ns (68.949%))

Logic Levels: 0

Clock Path Skew: 0.259ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.188ns

Source Clock Delay (SCD): 1.667ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.557 1.667 receiver/clk\_IBUF\_BUFG

SLICE\_X44Y97 FDCE r receiver/b\_reg\_reg[2]\_rep\_\_1/C

------------------------------------------------------------------- -------------------

SLICE\_X44Y97 FDCE (Prop\_fdce\_C\_Q) 0.141 1.808 r receiver/b\_reg\_reg[2]\_rep\_\_1/Q

net (fo=64, routed) 0.313 2.121 fifo\_rx/mem\_reg[769][7]\_0[2]

SLICE\_X52Y97 FDRE r fifo\_rx/mem\_reg[792][2]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.821 2.188 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X52Y97 FDRE r fifo\_rx/mem\_reg[792][2]/C

clock pessimism -0.261 1.926

SLICE\_X52Y97 FDRE (Hold\_fdre\_C\_D) 0.070 1.996 fifo\_rx/mem\_reg[792][2]

-------------------------------------------------------------------

required time -1.996

arrival time 2.121

-------------------------------------------------------------------

slack 0.125

Slack (MET) : 0.128ns (arrival time - required time)

Source: receiver/b\_reg\_reg[0]\_rep/C

(rising edge-triggered cell FDCE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Destination: fifo\_rx/mem\_reg[904][0]/D

(rising edge-triggered cell FDRE clocked by sys\_clk\_pin {rise@0.000ns fall@4.000ns period=10.000ns})

Path Group: sys\_clk\_pin

Path Type: Hold (Min at Fast Process Corner)

Requirement: 0.000ns (sys\_clk\_pin rise@0.000ns - sys\_clk\_pin rise@0.000ns)

Data Path Delay: 0.441ns (logic 0.141ns (31.981%) route 0.300ns (68.019%))

Logic Levels: 0

Clock Path Skew: 0.267ns (DCD - SCD - CPR)

Destination Clock Delay (DCD): 2.191ns

Source Clock Delay (SCD): 1.662ns

Clock Pessimism Removal (CPR): 0.261ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.243 0.243 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.842 1.084 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.026 1.110 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.552 1.662 receiver/clk\_IBUF\_BUFG

SLICE\_X52Y95 FDCE r receiver/b\_reg\_reg[0]\_rep/C

------------------------------------------------------------------- -------------------

SLICE\_X52Y95 FDCE (Prop\_fdce\_C\_Q) 0.141 1.803 r receiver/b\_reg\_reg[0]\_rep/Q

net (fo=64, routed) 0.300 2.103 fifo\_rx/mem\_reg[897][7]\_0[0]

SLICE\_X44Y95 FDRE r fifo\_rx/mem\_reg[904][0]/D

------------------------------------------------------------------- -------------------

(clock sys\_clk\_pin rise edge)

0.000 0.000 r

K17 0.000 0.000 r clk (IN)

net (fo=0) 0.000 0.000 clk

K17 IBUF (Prop\_ibuf\_I\_O) 0.431 0.431 r clk\_IBUF\_inst/O

net (fo=1, routed) 0.907 1.338 clk\_IBUF

BUFGCTRL\_X0Y16 BUFG (Prop\_bufg\_I\_O) 0.029 1.367 r clk\_IBUF\_BUFG\_inst/O

net (fo=16716, routed) 0.824 2.191 fifo\_rx/clk\_IBUF\_BUFG

SLICE\_X44Y95 FDRE r fifo\_rx/mem\_reg[904][0]/C

clock pessimism -0.261 1.929

SLICE\_X44Y95 FDRE (Hold\_fdre\_C\_D) 0.046 1.975 fifo\_rx/mem\_reg[904][0]

-------------------------------------------------------------------

required time -1.975

arrival time 2.103

-------------------------------------------------------------------

slack 0.128

Pulse Width Checks

--------------------------------------------------------------------------------------

Clock Name: sys\_clk\_pin

Waveform(ns): { 0.000 4.000 }

Period(ns): 10.000

Sources: { clk }

Check Type Corner Lib Pin Reference Pin Required(ns) Actual(ns) Slack(ns) Location Pin

Min Period n/a BUFG/I n/a 2.155 10.000 7.845 BUFGCTRL\_X0Y16 clk\_IBUF\_BUFG\_inst/I

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[0]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[1]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[2]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[3]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[4]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[5]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[6]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[7]/C

Min Period n/a FDRE/C n/a 1.000 10.000 9.000 SLICE\_X36Y87 fifo\_rx/mem\_reg[0][0]/C

Low Pulse Width Slow FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[0]/C

Low Pulse Width Fast FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[0]/C

Low Pulse Width Slow FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[1]/C

Low Pulse Width Fast FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[1]/C

Low Pulse Width Slow FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[2]/C

Low Pulse Width Fast FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[2]/C

Low Pulse Width Slow FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[3]/C

Low Pulse Width Fast FDRE/C n/a 0.500 6.000 5.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[3]/C

Low Pulse Width Slow FDRE/C n/a 0.500 6.000 5.500 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[4]/C

Low Pulse Width Fast FDRE/C n/a 0.500 6.000 5.500 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[4]/C

High Pulse Width Slow FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[0]/C

High Pulse Width Fast FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[0]/C

High Pulse Width Slow FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[1]/C

High Pulse Width Fast FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[1]/C

High Pulse Width Slow FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[2]/C

High Pulse Width Fast FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[2]/C

High Pulse Width Slow FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[3]/C

High Pulse Width Fast FDRE/C n/a 0.500 4.000 3.500 SLICE\_X53Y104 fifo\_rx/data\_out\_reg[3]/C

High Pulse Width Slow FDRE/C n/a 0.500 4.000 3.500 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[4]/C

High Pulse Width Fast FDRE/C n/a 0.500 4.000 3.500 SLICE\_X52Y103 fifo\_rx/data\_out\_reg[4]/C